A many-objective circuit design problem: The anti-alliasing filter

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Grundfos Technical Report 2009-01

1 Description of the Task

The task is to find component values for an anti-aliasing filter, which is a part of the motor control electronic circuitry for the Alpha Pro project.

The following components are predetermined for the application:

-TLC2272AC op-amp

-LPRC201 low-ohmic power chip resistor of the value of 300 mΩ and 1% tolerance

-a list of preferred values for resistors (1% tolerances) and capacitors (5% or 10% tolerances), SMD 0603.

A **single power supply** of **5 V** has also been predetermined.

2 Circuit Design by Optimization

In this project, an optimization algorithm was employed to determine the resistor and capacitor values of the circuits subjected to design. To apply optimization, a number of objectives have to be defined. Such objectives mathematically express the designer's requirements to the circuit's behavior. On an abstract level, one objective may be described as "achieve a lowpass-filter with cut-off frequency between 2 and 5Hz". This is then transformed to a mathematical function expressing the deviation between the actual and the desired AC-characteristics at a number of frequencies. The function has a minimum of zero indicating a perfect match between actual and desired AC-characteristics. The optimization algorithm minimizes the function to achieve the desired behavior.

Performing circuit design with an optimization algorithm has several advantages over other design methods:

- The algorithm uses values only from pre-specified component lists, e.g., resistors from the E96-row and capacitors from the E24-row. In manual design, it can be difficult to find standard component values yielding a solution that match the requirements.

- The algorithm can simultaneously handle several conflicting design objectives. In design without optimization, it may be difficult to find a good compromise when 5-10 objectives are considered simultaneously.

- The algorithm performs a broad exploration of the design space thereby providing several alternatives to be further investigated by the designer.

3 Circuit Configurations

The overall configuration consisting of the anti-aliasing filter is shown in Figure 1. The Differential Measurement circuit was predetermined in the project. In addition, the figure shows the block output voltage levels for each block, which illustrates the most important design requirements and limitations.

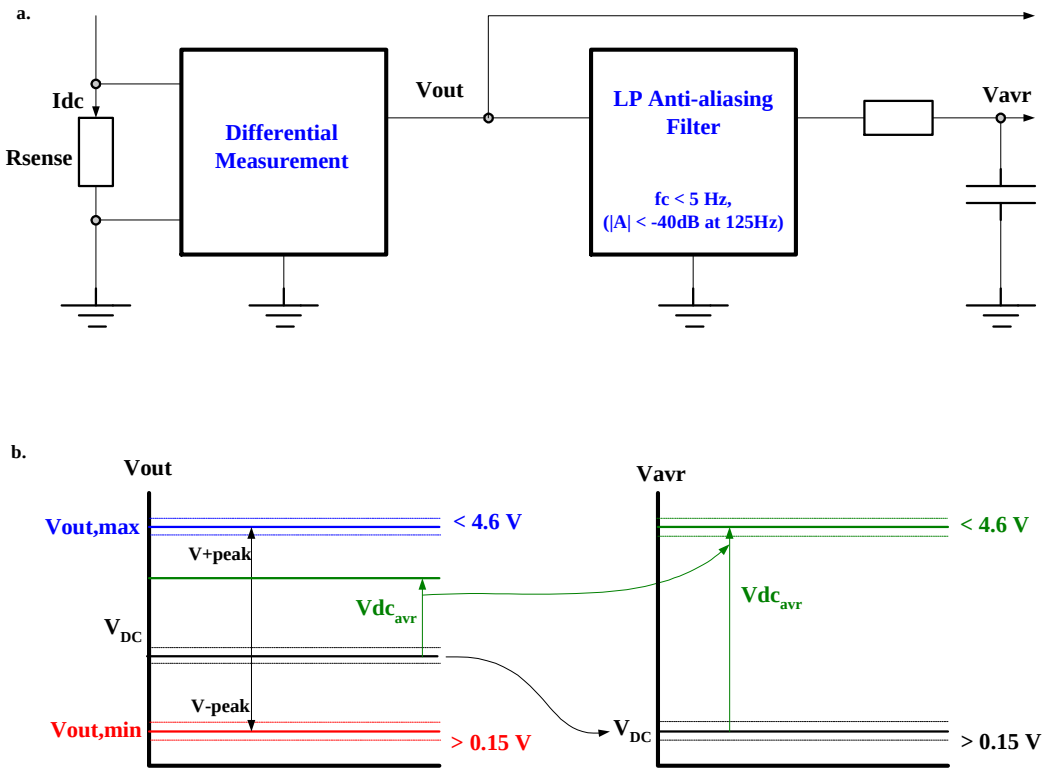

Figure 1. The overall configuration. a – The block diagram. b – The voltage levels at the block outputs.

3.1 The Anti-aliasing Filter

The filter is connected in cascade to the Differential Measurement circuit. Thus, the output signal of the Differential Measurement circuit constitutes the input signal of the filter.

3.1.1 The Specifications and Requirements

The average value of Idc, $\boldsymbol{Idc_{avr}}$ **= 0.3 A**.

The AC – functionality of the circuit is to provide low-pass filtering of Idc. The requirement for the magnitude characteristic *M(f)* is

Equation 1

$$20 \cdot \log\left(\frac{M(125Hz)}{M(0Hz)}\right) \leq -40\ dB\,.$$

The DC – functionalities of the circuit are to attenuate V_{DC} as much as possible and to amplify simultaneously the DC-component, i.e., the average value of the signal as much as possible. The limits for the two DC-functionalities are of course the low-level output voltage of the TLC2272AV op-amp at one and V_{ref} at the other end (see Figure 1b).

3.1.2 The configuration

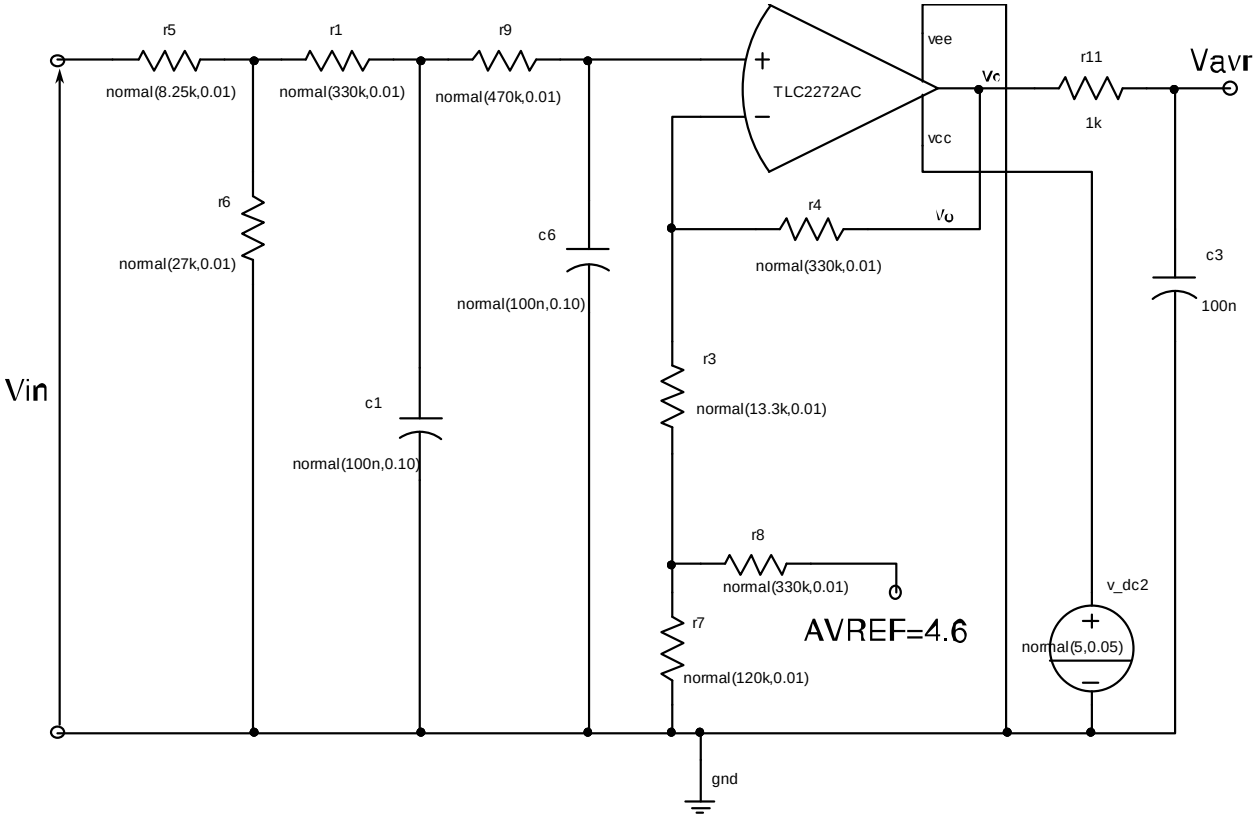

Figure 2. A second order RC-configuration with gain as the anti-aliasing filter.

A second order RC-configuration has been chosen for the purpose rather then the Sallen-Key circuit, because the magnitude characteristic of the latter is very sensitive to component value variations, especially in the stop-band.

The DC-component of the input signal *Vin* can be expressed as

Equation 2

$$Vin_{DC} = V_{DC} + Vdc_{avr},$$

where

Equation 3

$$Vdc_{avr} = Idc_{avr} \cdot Rsense \cdot G_{diff}.$$

The input range of the TLC2272AC op-amp is specified as **0 to VCC-1.5 V**. To prevent the op-amp from saturating for Vin_{DC} > VCC-1.5 a voltage divider r5, r6 is provided at the input of the circuit.

The components r1, r3, r4, r5, r6, r7, r8, r9, c1, c6 are subject to optimization. In the circuit of Figure 2 there are two additional passive components, r11 and c3. Their functionality is to form an interface to the A/D converter and as such their values are predetermined and not subjects to the filter design process.

3.1.3 The Equations and Requirements for the Optimization Purposes

For the purposes of DC-analysis of the circuit from Figure 2 we have

Equation 4

$$V_{avr} = \frac{1+\frac{r4}{r_{TOT}}}{1+\frac{r5}{r6}} \cdot \left(V_{DC} + Vdc_{avr}\right) - \frac{r4}{r_{TOT}} \cdot \frac{4.6}{1+\frac{r8}{r7}},$$

where

Equation 5

$$r_{TOT} = r3 + \frac{r7 \cdot r8}{r7 + r8}.$$

It is evident from Equation 4 that the positive term with V_{DC} in the equation can be reduced to the desired value by the negative term without inflicting the gain of Vdc_{avr}.

However, as it is indicated by means of the stipple lines in Figure 1 the values of V_{DC} and V_{avr} vary due to component tolerances. Thus, we have to

1. reduce the minimum value of V_{DC}, $V_{DC,\min}$, to 0.15 V and
2. gain the max value of $(V_{DC} + Vdc_{avr})$, $(V_{DC} + Vdc_{avr})_{\max}$, to 4.6 V.

This leaves us with the following equations

Equation 6

$$\frac{1+\frac{r4}{r_{TOT}}}{1+\frac{r5}{r6}} \cdot \left(V_{DC} + Vdc_{avr}\right)_{\max} - \frac{r4}{r_{TOT}} \cdot \frac{4.6}{1+\frac{r8}{r7}} = 4.6 - \Delta V1$$

corresponding to the requirement 1 and

Equation 7

$$\frac{1+\frac{r4}{r_{TOT}}}{1+\frac{r5}{r6}} \cdot V_{DC,\min} - \frac{r4}{r_{TOT}} \cdot \frac{4.6}{1+\frac{r8}{r7}} = 0.15 + \Delta V2$$

corresponding to requirement 2, where

Equation 8

$$G_{DC} = \frac{1+\frac{r4}{r_{TOT}}}{1+\frac{r5}{r6}}.$$

To assure realization of both requirements we set the following condition

Equation 9

$$\frac{r4}{r_{TOT}} = \frac{r6}{r5}.$$

Substituting Equation 9 into Equation 8, Equation 6 and Equation 7 results in the following modification of the two above mentioned requirements, i.e., Equation 6 and Equation 7, respectively.

Equation 10

$$G_{DC} \cdot \left(V_{DC} + Vdc_{avr}\right)_{\max} - G_{DC} \cdot \frac{4.6}{1+\frac{r8}{r7}} = 4.6 - \Delta V1$$

and

Equation 11

$$G_{DC} \cdot V_{DC,\min} - G_{DC} \cdot \frac{4.6}{1+\frac{r8}{r7}} = 0.15 + \Delta V2\,.$$

$V_{DC,\min}$ and $(V_{DC} + Vdc_{avr})_{\max}$ have been found by means of Monte Carlo analysis performed on the circuit for measurement of Idc. The values are found to be: $V_{DC,\min}$ = 1.301V and $\left(V_{DC} + Vdc_{avr}\right)_{\max}$ = 2.603V.

The variables ***ΔV1*** and ***ΔV2*** in the above equation are positive numbers. Their role in the nominal design is to provide the necessary margins for component variations (in this case - 6σ approach). They are found in an iterative process of successive circuit optimization and Monte Carlo analysis.

Notice that r1, r9, r11, c1, c3 and c6 (see Figure 2) have no influence on the DC-functionality of the circuit under consideration.

On the other hand, those components together with the rest of the resistors determine the AC-functionality of the circuit, the low-pass filtering of the signal with the cut-off frequency between $2\,Hz \le f_C \le 5\,Hz$. The components r1, r9, c1 and c6 have also been found by means of the same optimization procedure, in this part based on AC analysis in SABER.

For the optimization, a number of objectives must be defined. The AC-functionality is reformulated as the minimization of two functions. Equation 12 ensures that the filter has a cut-off frequency between 2 and 5*Hz*, whereas Equation 13 promotes maximal dampening at 125*Hz*.

Equation 12

$$ACappr = \sum_{f_i} \begin{cases} 20\log(M(f_i)) - v_{i,\max} & 20\log(M(f_i)) > v_{i,\max} \\ v_{i,\min} - 20\log(M(f_i)) & 20\log(M(f_i)) < v_{i,\min} \\ 0 & \text{Otherwise} \end{cases}$$

where $M(f_i)$ is the magnitude in dB and the frequencies and interval values are as in Table 1. The *ACappr* objective has a minimum of zero when the circuit has the desired filter characteristics, i.e, that the magnitude is between $v_{i,\min}$ and $v_{i,\max}$ at the specified frequencies.

f_i	$v_{i,\min}$	$v_{i,\max}$	**Comments**
0.01	8.5	10.63	Lifts AC-characteristic to desired level
2	6.42	10.63	Min 2Hz filter
5	0.42	7.63	Max 5Hz filter

Table 1: Frequencies and magnitudes (dB) for AC-approximation.

Maximal dampening at 125*Hz* is achieved by minimizing the slope around 40-50*Hz*.

Equation 13

$$Slope = \frac{20\log(M(f_2)) - 20\log(M(f_1))}{f_2 - f_1}$$

where f_1=40*Hz* and f_2=50*Hz*.

The DC-rescale is achieved by minimizing three functions, *GainDevi*, *DCMax* and *DCMin*, which are reformulations of Equation 9, Equation 6 and Equation 7, respectively.

The three functions are

Equation 14

$$GainDevi = abs\left(1.0 - \frac{r6}{r5} \cdot \frac{r_{TOT}}{r4}\right),$$

Equation 15

$$DCMax = abs(4.6 - \Delta V1 - V_{\max})$$

and

Equation 16

$$DCMin = abs(0.15 + \Delta V2 - V_{\min})$$

where (see Equation 6 and Equation 7)

Equation 17

$$V_{\max} = \frac{1+\frac{r4}{r_{TOT}}}{1+\frac{r5}{r6}} \cdot \left(V_{DC} + Vdc_{avr}\right)_{\max} \quad \text{and} \quad V_{\min} = \frac{1+\frac{r4}{r_{TOT}}}{1+\frac{r5}{r6}} \cdot V_{DC,\min} .$$

In addition to the objective, a number of constraints must be satisfied to ensure a valid circuit. The constraints are listed in Table 2.

Constraint	Comments
$r5 + r6 \geq 23000\Omega$	Ensures minimum value of the circuit's input impedance
$r7 \geq 10000\Omega$	Limits the current consumption from AVREF (Figure 2)
$c6 \leq 100nF$	Practical limitation on the capacitor value
$r9 \leq 500k\Omega$	Practical limitation on the resistor value

Table 2: Constraints.

4 Available components

In a total view of the project, it is desirable to limit the set of available components to those actually in stock. This is desirable since a rather large startup price and also annual costs are a result of introducing additional components. Furthermore, the SMD components are supplied on tapes and the SMD-mounting robots have a max width of 60cm on the production feeder. Thus limiting the number of new components will also help reducing costs in production since it may be necessary to extend the production line with an additional feeder (costs approx 100k Euro).

22	390	1.05k	4.7k	12.0k	27.0k	62.0k	165k	680k
47	470	1.2k	6.8k	13.3k	33.0k	64.9k	200k	976k
82	590	2.2k	8.25k	15.0k	38.3k	100k	205k	1meg
150	680	2.7k	9.1k	20.0k	44.2k	118k	330k	
220	887	3.0k	10.0k	22.0k	47.0k	120k	422k	
330	1.0k	3.74k	10.5k	24.9k	56.0k	124k	470k	

Table 3: List of resistors in stock (all 1% tolerance).

15p	82p	220p	1n	27n	47n
22p	100p	330p	4.7n	33n	56n
33p	150p	470p	22n	39n	100n

Table 4: List of capacitors in stock (all 5% tolerance).